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XBERT Device
Bit Error Rate Generator Receiver
TXC-06125

DATA SHEET
Preliminary

FEATURES

- Serial, nibble, or byte wide interface capability
- Transmit and receive clock rate: 100 Hz to 52.00 MHz (serial, byte, nibble I/O) (All telecom rates up to STS-3)
- Up to 414.72 Mbit/s test patterns using the byte-wide interface and some external circuitry
- $2^{15} - 1$, $2^{20} - 1$, $2^{20} - 1$ QRSS, $2^{23} - 1$ pseudorandom generators and detectors
- Fixed word test generators and detectors
  - All ones
  - All zeros
  - Alternate 1/0 pattern
  - Double 1/0 pattern
- Microprocessor programmable test word generator and detector (up to 32 bits)
- Error rate generators (single, 10^{-3} and 10^{-6})
- Bit error counter and bit counter (24 bits each)

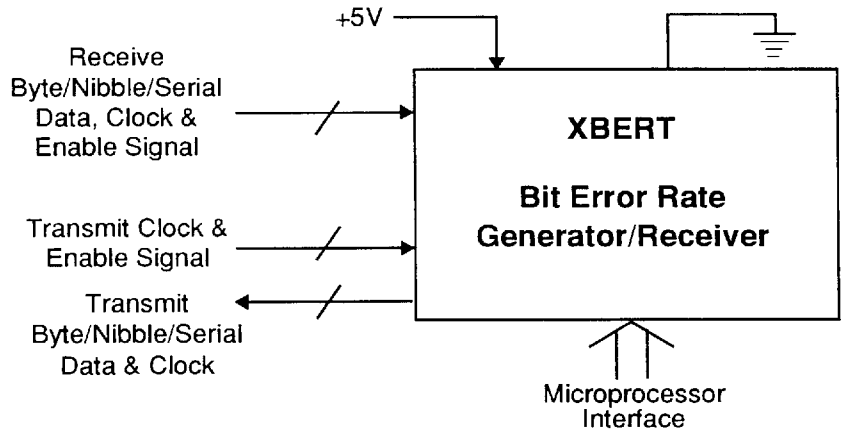
DESCRIPTION

The Bit Error Rate Generator/Receiver (XBERT) is a programmable (via microprocessor) multi-rate test pattern generator and receiver on a single chip. It is used for testing the performance of digital communication circuits and communication links and supports a bit-serial, nibble-parallel or byte-parallel interface. The XBERT is capable of operating in a burst data mode by using an external enable signal to enable/disable the transmit and receive clock. The XBERT generates and analyzes pseudorandom patterns, fixed words, or programmable words. Four pseudorandom test patterns are provided: $2^{15} - 1$, $2^{20} - 1$, $2^{20} - 1$ with zero suppression (QRSS)*, and $2^{23} - 1$. The fixed word mode generates and analyzes all zeros, all ones, alternate one/zero pattern or a double alternate one/zero (1100) pattern. The programmable mode allows a choice of one to four bytes written by the microprocessor.

*2^{20} -1 Quasi-Random Signal Source not available in byte-wide mode.

APPLICATIONS

- Transmission and switching systems
- Data communications
- Test equipment
- Remote testing and fault isolation
- Embedded test for proprietary framing algorithms
- Embedded test for secure lines



Patents Pending
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BLOCK DIAGRAM

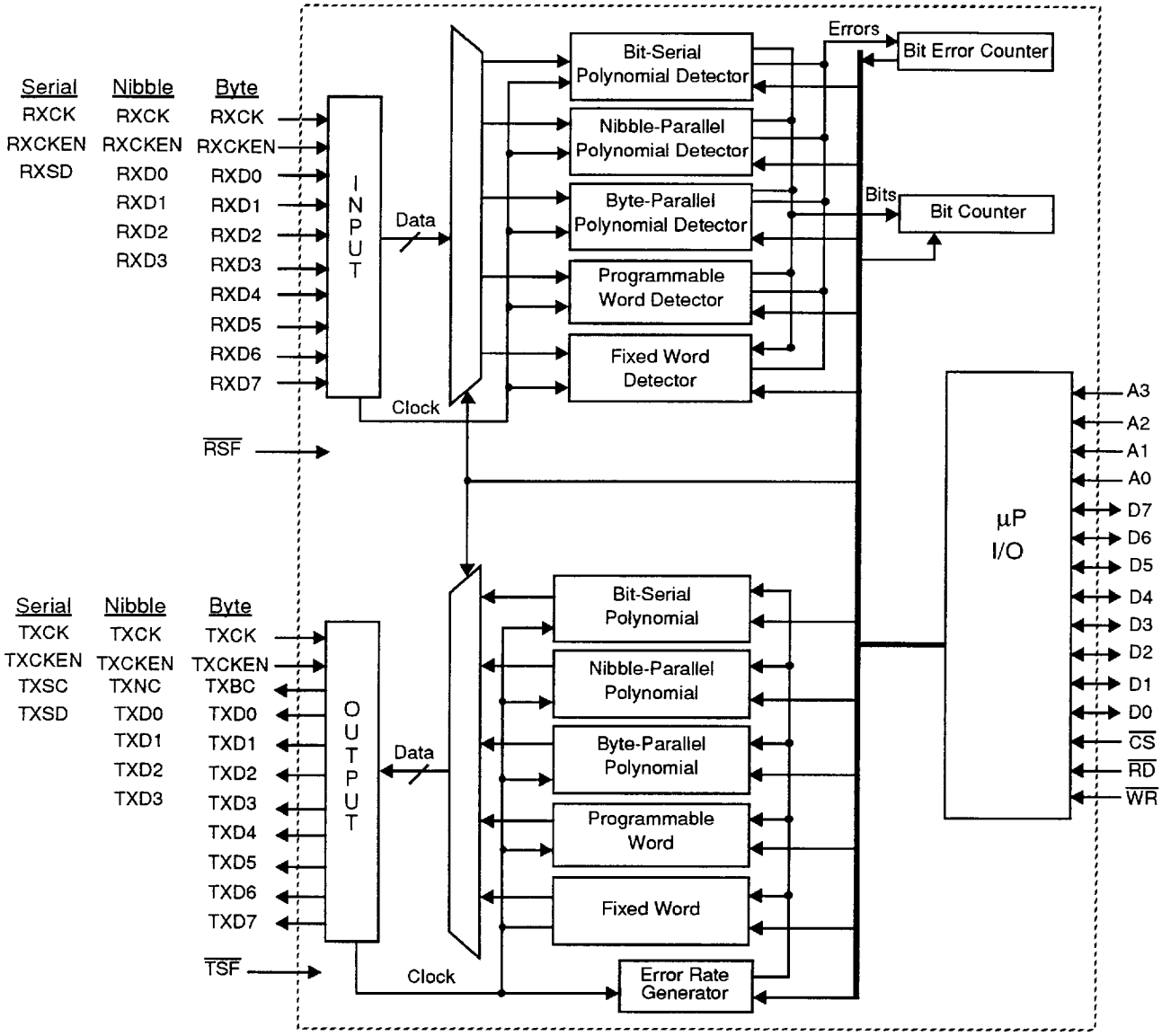

Figure 1. XBERT Block Diagram

BLOCK DIAGRAM DESCRIPTION

Figure 1 is a simplified block diagram of the XBERT and its signal leads. The Input Block accepts bit-serial (RXSD), nibble-parallel (RXD3-0) or byte-parallel (RXD7-0) data, which is selected by writing control bits in the memory map. Incoming data is clocked into the XBERT on positive transitions of the clock signal (RXCK). An input for a receive enable signal (RXCKEN) is provided. An active low on this signal lead disables the input clock from clocking in data.

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The test pattern, which is common to both the receiver and transmitter, is selected by writing control bits in the memory map. Each of the test pattern detectors is equipped with a pattern generator and comparator. The comparison between the incoming data and the test generator is enabled after frame alignment takes place, or when the receive start of the pseudorandom feature ($\overline{RSF}$) is used.

A simplified view of the frame alignment, detecting errors and loss of frame alignment for a 1100 pattern is shown below:

	start	in frame check	OOF				OOF
Received signal	1100110011001100			1100100011101101	1100		
Local generated signal		11001101		1100110011001100			
Detected errors			1	1	1	1	

A running count of the number of bit errors and bit counts is stored in two 24-bit counters. Bit error rate performance is determined by having the microprocessor read the counter on a scheduled basis and compute the error rate.

The transmit clock signal (TXCK) provides the time base for transmitter operation. An input transmit enable signal (TXCKEN) is provided. An active low disables the input clock (TXCK). This feature is provided for applications where a gapped clock signal is required to prevent the transmitter from clocking out test pattern data.

The interface selection is common for both the receiver and transmitter. The transmit clock signal (TXCK) is also used to clock the nibble-parallel (TXD3-0) and byte-parallel data (TXD7-0) out of the XBERT. Data is clocked out of the XBERT on negative transitions of the clock. The transmit clock signal (TXCK) is used to derive the serial clock signal (TXSC). The serial clock signal is used to clock serial data out of the XBERT on negative transitions.

For framer applications, a transmit start of pseudorandom pattern pulse ($\overline{TSF}$) is used to preset the transmit pseudorandom generators' shift registers to ones. This feature permits the XBERT to immediately start the pseudorandom pattern with a fixed relationship with the start of a frame.

For framer applications, a receive start of pseudorandom pattern pulse ($\overline{RSF}$) disables the frame alignment circuits in the pseudorandom detectors and presets the detector pseudorandom generators' shift registers to ones. Used in conjunction with the transmit start of pseudorandom pattern pulse, this feature permits the XBERT to immediately start a search for bit errors in the receive data. A software reset is required to enable the frame alignment circuitry in the pseudorandom detectors for normal operation.

The microprocessor interface consists of four address bits (A3-0), eight bidirectional data bus bits, chip select ($\overline{CS}$), and the read ($\overline{RD}$) and write ($\overline{WR}$) signal inputs. A transmit loopback feature is provided for self-testing the XBERT device.

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PIN DIAGRAM

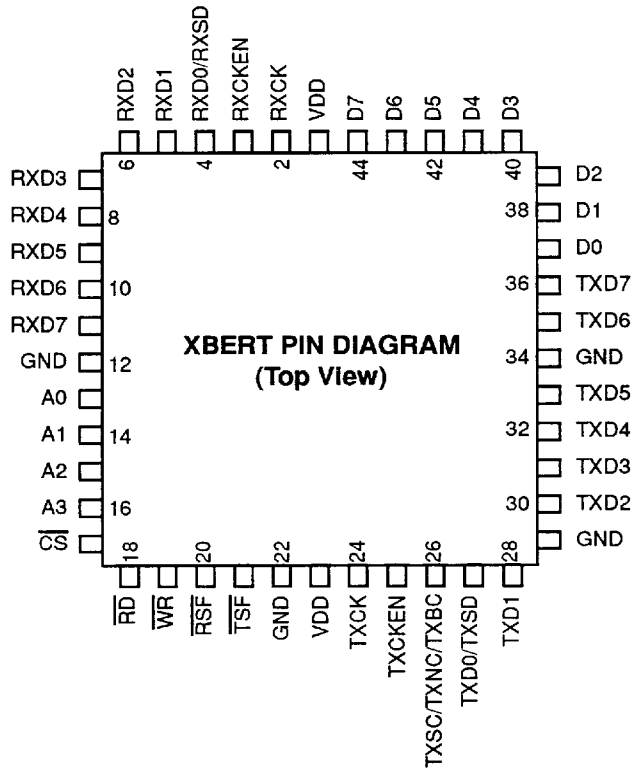

Figure 2. XBERT Pin Diagram With Names and Numbers

PIN DESCRIPTIONS

Power Supply and Ground

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	1, 23	P		**VDD:** 5 volt supply ±5%
GND	12, 22 29, 34	P		**Ground.**

*Note: I = Input; O = Output; P = Power

Receive Interfaces

Symbol	Pin No.	I/O/P	Type	Name/Function
RXCK	2	I	TTLp	**Receive Clock:** Bit-serial, nibble-parallel, and byte-parallel receive data is clocked into the XBERT on the rising edge of this clock. This clock is used as the time base for all receive functions. It may be gapped to accommodate overhead bit times. Loss of this clock causes the XBERT receiver to become inoperative.
RXCKEN	3	I	TTLp	**Receive Clock Enable:** A high enables the receive clock for clocking data into the XBERT. A low disables the clock from clocking in receive bit-serial, nibble-parallel, or byte-parallel data.

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Symbol	Pin No.	I/O/P	Type	Name/Function
RXD0/RXSD	4	I	TTLp	**Receive Nibble/Byte-Parallel Data Bit 0/Receive Serial Data:** This bit is the least significant bit for receive nibble/byte-parallel data. This pin is also shared as the input pin for serial data.
RXD1	5	I	TTLp	**Receive Nibble/Byte-Parallel Data Bit 1.**
RXD2	6	I	TTLp	**Receive Nibble/Byte-Parallel Data Bit 2.**
RXD3	7	I	TTLp	**Receive Nibble/Byte-Parallel Data Bit 3:** This bit is the most significant bit for the nibble-parallel interface.
RXD4	8	I	TTLp	**Receive Byte-Parallel Data Bit 4.**
RXD5	9	I	TTLp	**Receive Byte-Parallel Data Bit 5.**
RXD6	10	I	TTLp	**Receive Byte-Parallel Data Bit 6.**
RXD7	11	I	TTLp	**Receive Byte-Parallel Data Bit 7:** This bit is the most significant bit for the byte-parallel interface.
$\overline{\text{RSF}}$	20	I	TTLp	**Receive Start of Pseudorandom Pattern Framing:** An active low, one clock cycle wide pulse which presets the pseudorandom generator in the detector to all ones, thus defining the start of the pattern detection. The first pulse disables the loss of frame alignment circuit, and enables the bit error counter and bit counter. The receive clock enable signal (RXCKEN) must be high when $\overline{\text{RSF}}$ is clocked in. Once enabled, this feature can only be disabled by a reset.

Transmit Interfaces

Symbol	Pin No.	I/O/P	Type	Name/Function
TXCK	24	I	TTLp	**Transmit Clock:** An input clock used as the time base for generating the test patterns and for sourcing bit-serial, nibble-parallel, and byte-parallel transmit data out of the XBERT. This clock may be gapped to accommodate overhead bit times as required. Loss of this clock causes the transmit part of the XBERT to become inoperative.
TXCKEN	25	I	TTLp	**Transmit Clock Enable:** A high enables the transmit clock (TXCK) for clocking data out of the XBERT. A low disables the clock from clocking out transmit bit-serial, nibble-parallel, or byte-parallel data.
TXSC/ TXNC/ TXBC	26	O	TTL8mA	**Transmit Serial/Nibble/Byte Clock:** This clock is derived from the transmit clock signal (TXCK), and is used for clocking out data from the XBERT. Data is clocked out of the XBERT on the falling edge of this clock. This clock will have gapped periods corresponding to the time when the transmit enable signal (TXCKEN) is low.

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Symbol	Pin No.	I/O/P	Type	Name/Function
TXD0/TXSD	27	O	TTL8mA	**Transmit Nibble/Byte-Parallel Data Bit 0/Transmit Serial Data:** This bit is the least significant bit and the last bit clocked out of the XBERT for transmit nibble/ byte-parallel data. This pin is also used for transmit serial data.
TXD1	28	O	TTL8mA	**Transmit Nibble/Byte-Parallel Data Bit 1.**
TXD2	30	O	TTL8mA	**Transmit Nibble/Byte-Parallel Data Bit 2.**
TXD3	31	O	TTL8mA	**Transmit Nibble/Byte-Parallel Data Bit 3:** This bit is the most significant bit for the nibble-parallel interface.
TXD4	32	O	TTL8mA	**Transmit Byte-Parallel Data Bit 4.**
TXD5	33	O	TTL8mA	**Transmit Byte-Parallel Data Bit 5.**
TXD6	35	O	TTL8mA	**Transmit Byte-Parallel Data Bit 6.**
TXD7	36	O	TTL8mA	**Transmit Byte-Parallel Data Bit 7.** This bit is the most significant bit for the byte-parallel interface.
$\overline{TSF}$	21	I	TTLp	**Transmit Start of Pseudorandom Pattern Framing:** An active low, one clock cycle wide pulse which presets the transmit pseudorandom generator to all ones, thus defining the start of the transmitted test pattern. If the transmit clock enable signal (TXCKEN) is high when $\overline{TSF}$ is clocked in (positive clock transition), the generator transmits the start of the pseudorandom test pattern one and one-half clock cycles later (negative clock transition).

Microprocessor Interfaces

Symbol	Pin No.	I/O/P	Type	Name/Function
D(7-0)	44-37	I/O	TTL8mA	**Data Bus:** Used for programming and reading the registers which reside in the XBERT. The most significant bit is D7.
$\overline{CS}$	17	I	TTLp	**Chip Select:** A low enables data transfers between the microprocessor and the XBERT memory map during a read/write bus cycle.
$\overline{RD}$	18	I	TTLp	**Read Data:** An active low signal generated by the microprocessor for reading the registers which reside in the memory map. The XBERT memory I/O is selected by placing a low on the chip select lead.
$\overline{WR}$	19	I	TTLp	**Write Data:** An active low signal generated by the microprocessor for writing to the registers which reside in the memory map. The XBERT memory I/O is selected by placing a low on the chip select lead.
A(3-0)	16-13	I	TTLp	**Address Lines:** The four address lines are used to select an XBERT register location.

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ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	7	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous power dissipation	P_C		500	mW
Ambient operating temperature	T_A	**	**	°C
Operating junction temperature	T_J		125	°C
Storage temperature range	T_S	-55	125	°C

*Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

**Ambient operating temperature will be dependent on the total thermal analysis.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal res - junc to ambient			68	°C/W	
Thermal res - junc to case		22		°C/W	

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5	5.25	V	
I_{DD}			*	mA	
P_{DD}			*	mW	Inputs switching

*Power dissipation is application specific. See power vs. frequency graph, Figure 3, on page 8.

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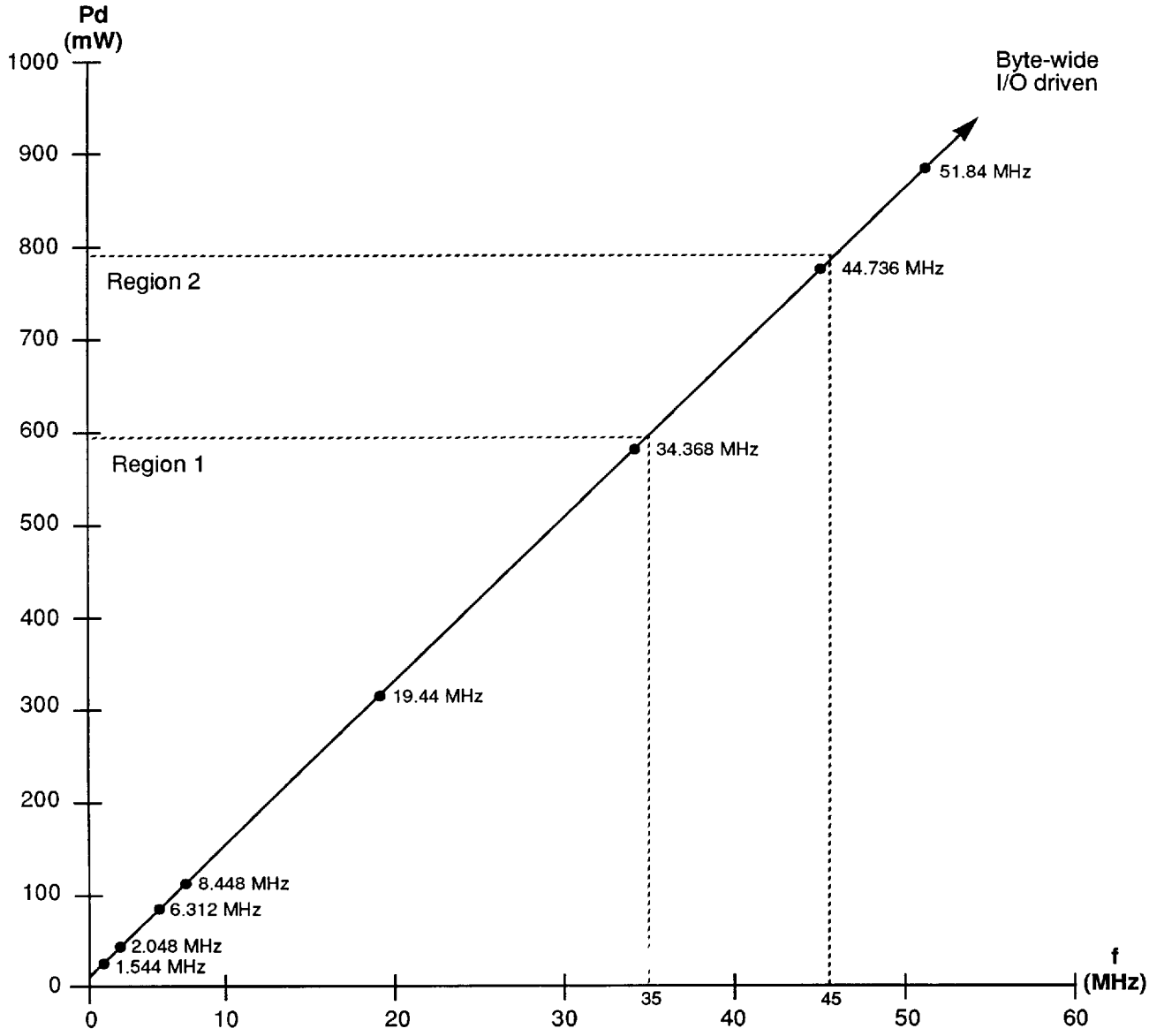
Safe Operating Regions Defined By Equation:
$T_{JMAX} = T_A + 68°C/W\ (Pd)$



Region 1 = XBERT may be used in a maximum ambient temperature of 85°C for TXCK and RXCK clock frequencies ≤ 35 MHz. This yields a maximum bit rate of 8 x 35 = 280 Mbit/sec.

Region 2 = XBERT may be used in a maximum ambient temperature of 70°C for TXCK and RXCK clock frequencies 35 MHz ≤ f ≤ 45 MHz. This yields a maximum bit rate of 8 x 45 = 360 Mbit/sec.

Note: Combinations of frequency and ambient temperature beyond the safe operating regions require additional heat dissipation methods.

Figure 3. Power Dissipation As A Function of Frequency

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INPUT, OUTPUT, AND I/O PARAMETERS

Input Parameters For TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		-70.0		µA	$V_{DD} = 5.25$
Input capacitance		3.79		pF	

Note: Input has a 72k (nominal) internal pullup resistor.

Output Parameters For TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	3.7			V	$V_{DD} = 4.75$; $I_{OH} = -8.0$ mA
V_{OL}			0.5	V	$V_{DD} = 4.75$; $I_{OL} = 8.0$ mA
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}	1.05	2.65	5.64	ns	$C_{LOAD} = 15$ pF
t_{FALL}	2.74	6.11	11.71	ns	$C_{LOAD} = 15$ pF

Input/Output Parameters For TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		-70.0		µA	$V_{DD} = 5.25$
Input capacitance		7.13		pF	
V_{OH}	3.7			V	$V_{DD} = 4.75$; $I_{OH} = -8.0$ mA
V_{OL}			0.5	V	$V_{DD} = 4.75$; $I_{OL} = 8.0$ mA
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}	1.12	3.29	7.26	ns	$C_{LOAD} = 15$ pF
t_{FALL}	3.16	7.95	15.92	ns	$C_{LOAD} = 15$ pF

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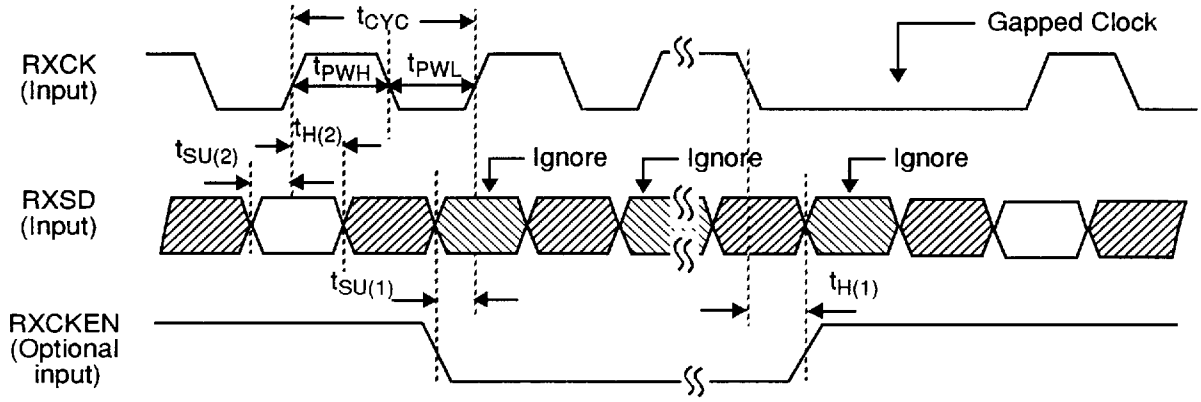
TIMING CHARACTERISTICS

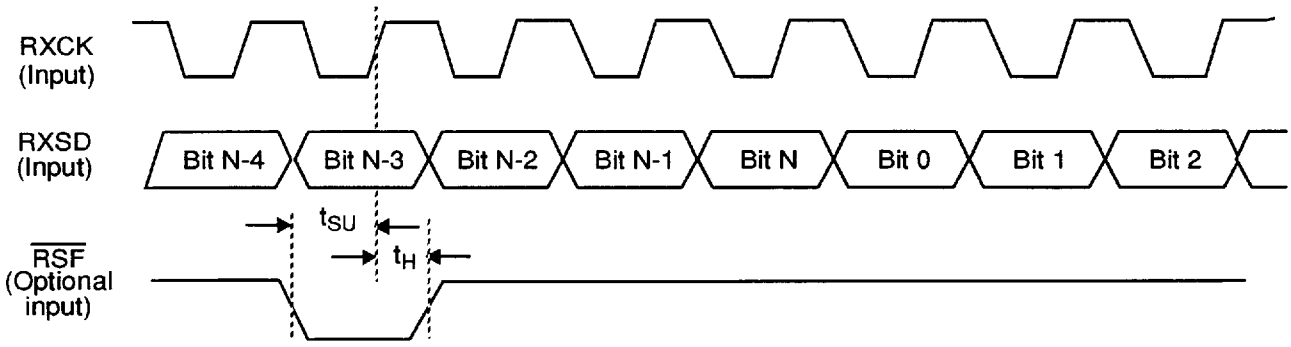
Detailed timing diagrams for the XBERT are illustrated in Figures 4 through 11, with values of the timing intervals following each figure. All output times are measured with a maximum 75 pF load capacitance. Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

Figure 4. Receive Serial Interface Timing



Parameter	Symbol	Min	Typ	Max	Unit
RXCK clock period	t_{CYC}	19.0			ns
RXCK high time	t_{PWH}	8.0	1/2 t_{CYC}		ns
RXCK low time	t_{PWL}	8.0	1/2 t_{CYC}		ns
RXCKEN set-up time to RXCK↑	$t_{SU(1)}$	2.5			ns
RXCKEN hold time after RXCK↓	$t_{H(1)}$	2.5			ns
RXSD set-up time to RXCK↑	$t_{SU(2)}$	3.0			ns
RXSD hold time after RXCK↑	$t_{H(2)}$	3.0			ns

Note: RXCK may be gapped or stretched without the use of the RXCKEN input to accommodate overhead bit times.



Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RSF}$ set-up time to RXCK↑	t_{SU}	2.5			ns
$\overline{RSF}$ hold time after RXCK↑	t_H	2.5			ns

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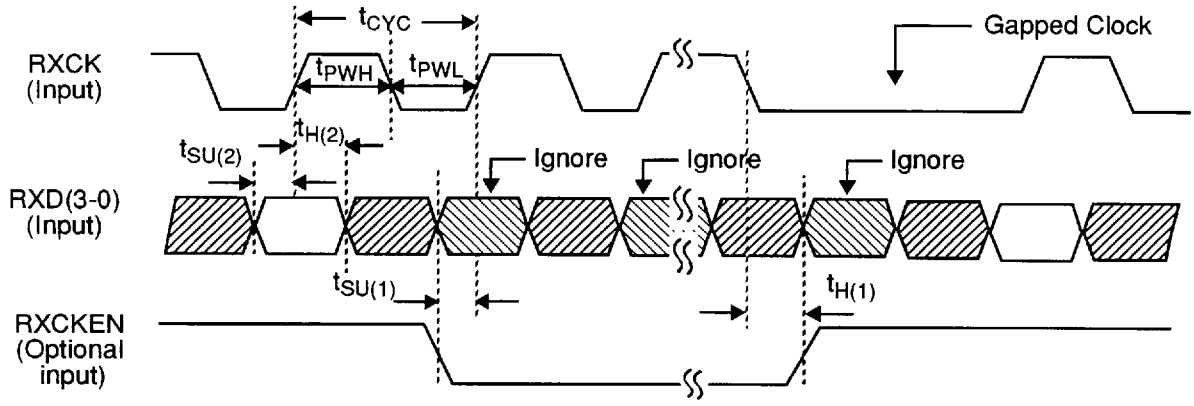
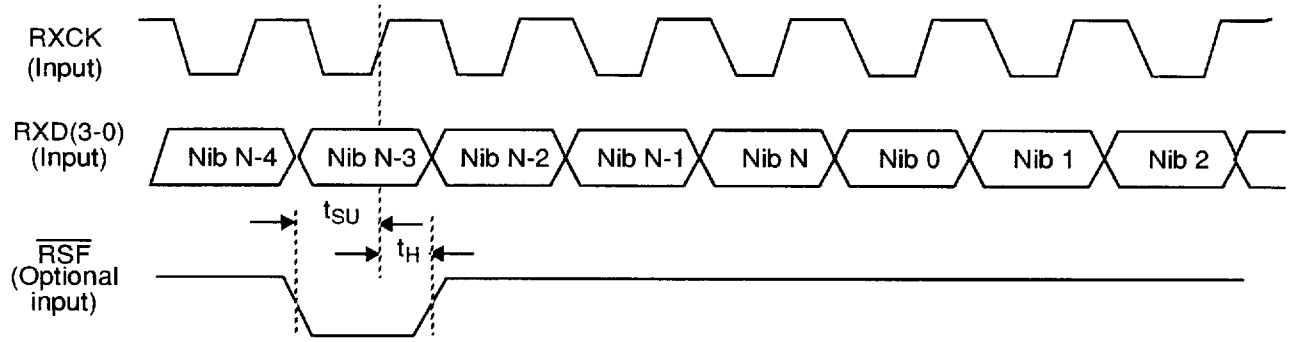
Figure 5. Receive Nibble Interface Timing



Parameter	Symbol	Min	Typ	Max	Unit
RXCK clock period	t_{CYC}	19.0			ns
RXCK high time	t_{PWH}	8.0	1/2 t_{CYC}		ns
RXCK low time	t_{PWL}	8.0	1/2 t_{CYC}		ns
RXCKEN set-up time to RXCK↑	$t_{SU(1)}$	2.5			ns
RXCKEN hold time after RXCK↓	$t_{H(1)}$	2.5			ns
RXD(3-0) set-up time to RXCK↑	$t_{SU(2)}$	3.0			ns
RXD(3-0) hold time after RXCK↑	$t_{H(2)}$	3.0			ns

Note: RXCK may be gapped or stretched without the use of the RXCKEN input to accommodate overhead bit times.



Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RSF}$ set-up time to RXCK↑	t_{SU}	2.5			ns
$\overline{RSF}$ hold time after RXCK↑	t_H	2.5			ns

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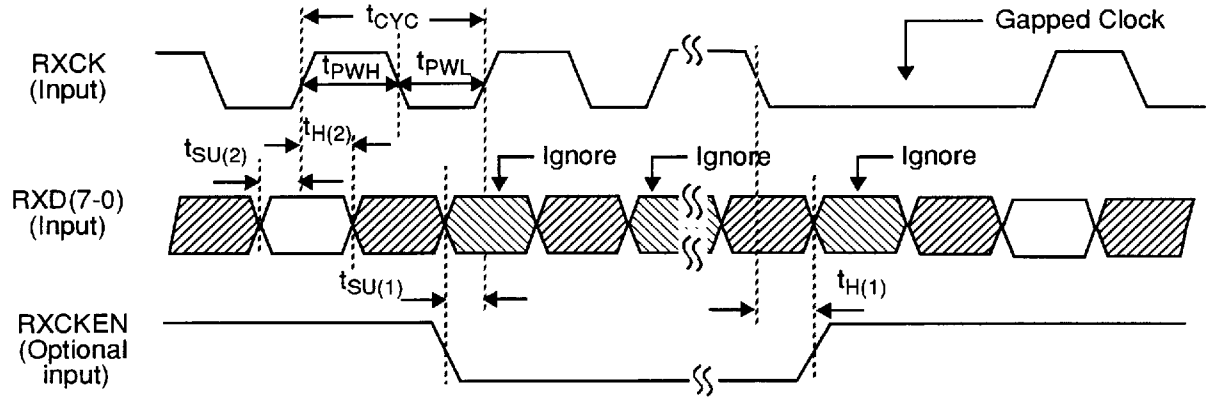
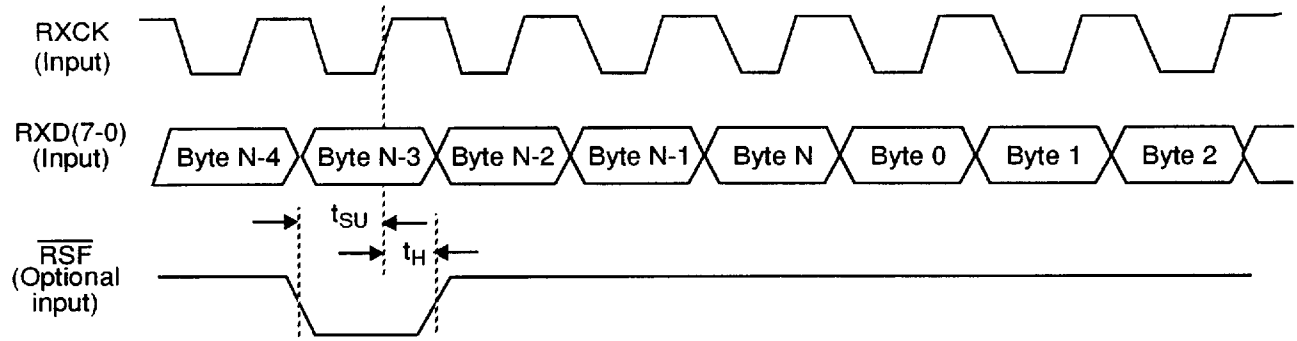
Figure 6. Receive Byte Interface Timing



Parameter	Symbol	Min	Typ	Max	Unit
RXCK clock period	t_{CYC}	19.0			ns
RXCK high time	t_{PWH}	8.0	1/2 t_{CYC}		ns
RXCK low time	t_{PWL}	8.0	1/2 t_{CYC}		ns
RXCKEN set-up time to RXCK↑	$t_{SU(1)}$	2.5			ns
RXCKEN hold time after RXCK↓	$t_{H(1)}$	2.5			ns
RXD(7-0) set-up time to RXCK↑	$t_{SU(2)}$	3.0			ns
RXD(7-0) hold time after RXCK↑	$t_{H(2)}$	3.0			ns

Note: RXCK may be gapped or stretched without the use of the RXCKEN input to accommodate overhead bit times.



Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RSF}$ set-up time to RXCK↑	t_{SU}	2.5			ns
$\overline{RSF}$ hold time after RXCK↑	t_H	2.5			ns

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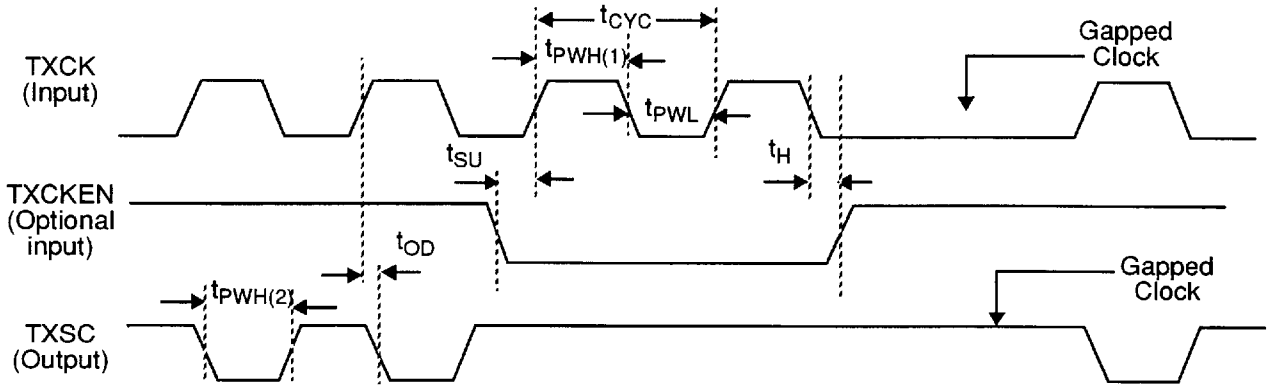
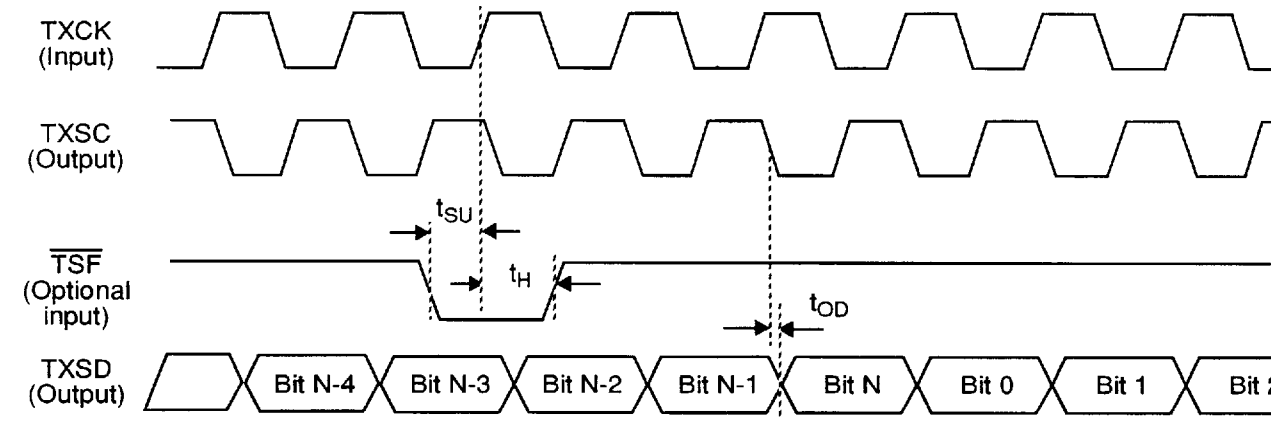
Figure 7. Transmit Serial Interface Timing



Parameter	Symbol	Min	Typ	Max	Unit
TXCK clock period	t_{CYC}	19.0			ns
TXCK high time	$t_{PWH(1)}$	8.0	1/2 t_{CYC}		ns
TXCK low time	t_{PWL}	8.0	1/2 t_{CYC}		ns
TXCKEN set-up time to TXCK↑	t_{SU}	2.5			ns
TXCKEN hold time after TXCK↓	t_H	2.5			ns
TXSC output delay after TXCK↑	t_{OD}			5.0	ns
TXSC high time	$t_{PWH(2)}$	7.6			ns

Note: The clock (TXCK) may be gapped or stretched without the use of TXCKEN to accommodate overhead bit times.



Parameter	Symbol	Min	Typ	Max	Unit
TXSD output delay after TXSC↓	t_{OD}			5.0	ns
$\overline{TSF}$ set-up time to TXCK↑	t_{SU}	2.5			ns
$\overline{TSF}$ hold time after TXCK↑	t_H	2.5			ns

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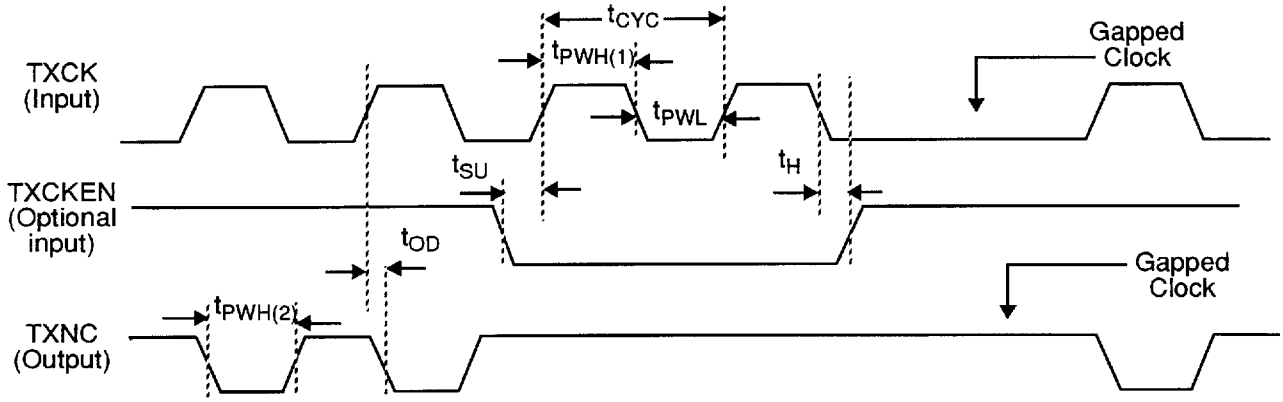
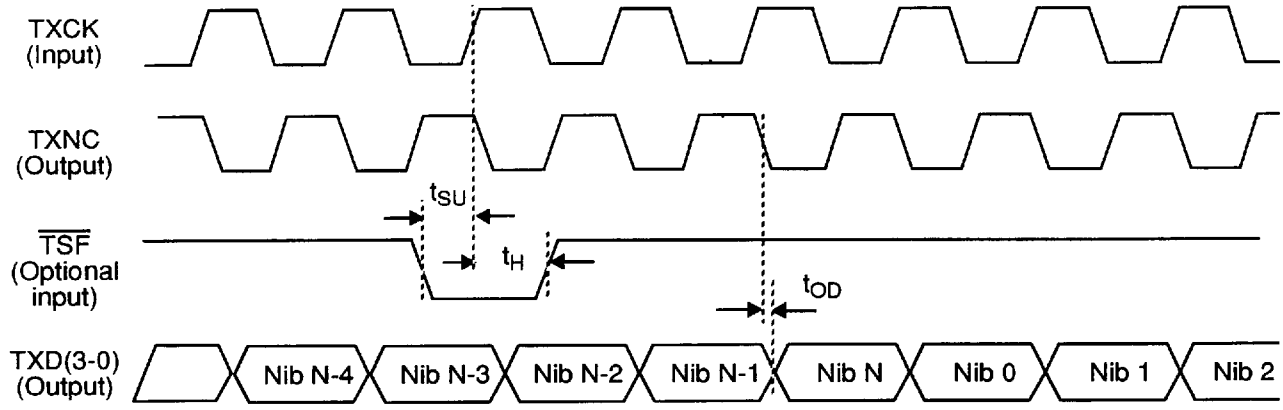
Figure 8. Transmit Nibble Interface Timing



Parameter	Symbol	Min	Typ	Max	Unit
TXCK clock period	t_{CYC}	19.0			ns
TXCK high time	$t_{PWH(1)}$	8.0	1/2 t_{CYC}		ns
TXCK low time	t_{PWL}	8.0	1/2 t_{CYC}		ns
TXCKEN set-up time to TXCK↑	t_{SU}	2.5			ns
TXCKEN hold time after TXCK↓	t_H	2.5			ns
TXNC output delay after TXCK↑	t_{OD}			5.0	ns
TXNC high time	$t_{PWH(2)}$	7.6			ns

Note: The clock (TXCK) may be gapped or stretched without the use of TXCKEN to accommodate overhead bit times.



Parameter	Symbol	Min	Typ	Max	Unit
TXD output delay after TXNC↓	t_{OD}			5.0	ns
$\overline{TSF}$ set-up time to TXCK↑	t_{SU}	2.5			ns
$\overline{TSF}$ hold time after TXCK↑	t_H	2.5			ns

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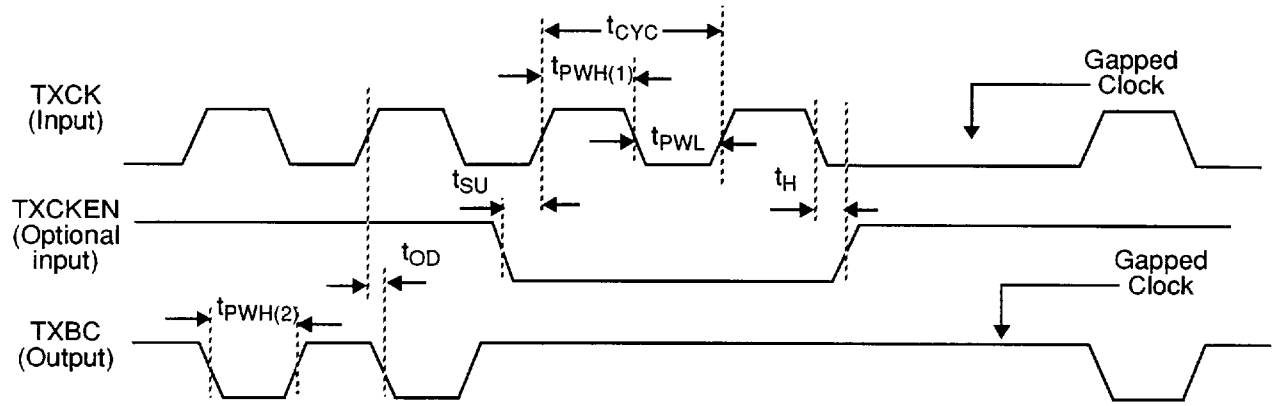
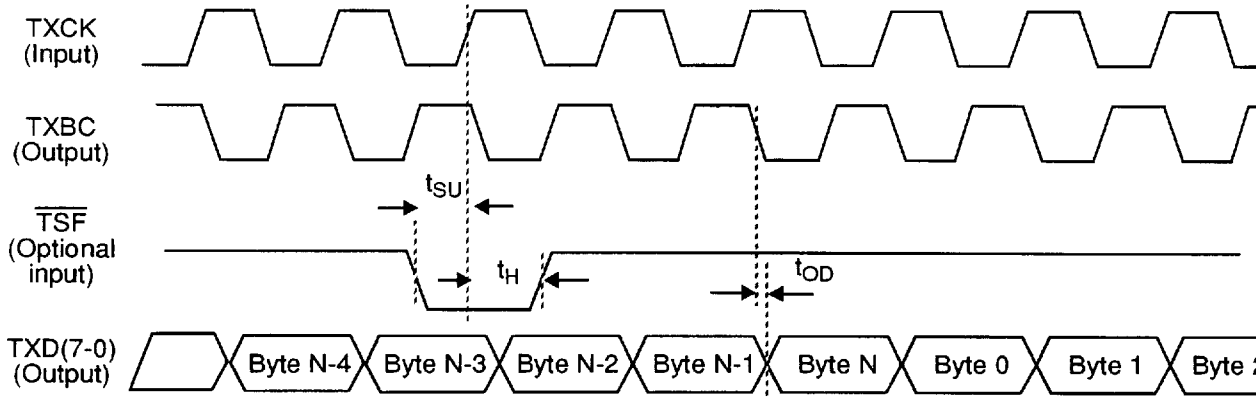
Figure 9. Transmit Byte Interface Timing



Parameter	Symbol	Min	Typ	Max	Unit
TXCK clock period	t_{CYC}	19.0			ns
TXCK high time	$t_{PWH(1)}$	8.0	1/2 t_{CYC}		ns
TXCK low time	t_{PWL}	8.0	1/2 t_{CYC}		ns
TXCKEN set-up time to TXCK↑	t_{SU}	2.5			ns
TXCKEN hold time after TXCK↓	t_H	2.5			ns
TXBC output delay after TXCK↑	t_{OD}			5.0	ns
TXBC high time	$t_{PWH(2)}$	7.6			ns

Note: The clock (TXCK) may be gapped or stretched without the use of TXCKEN to accommodate overhead bit times.



Parameter	Symbol	Min	Typ	Max	Unit
TXD output delay after TXBC↓	t_{OD}			5.0	ns
$\overline{TSF}$ set-up time to TXCK↑	t_{SU}	2.5			ns
$\overline{TSF}$ hold time after TXCK↑	t_H	2.5			ns

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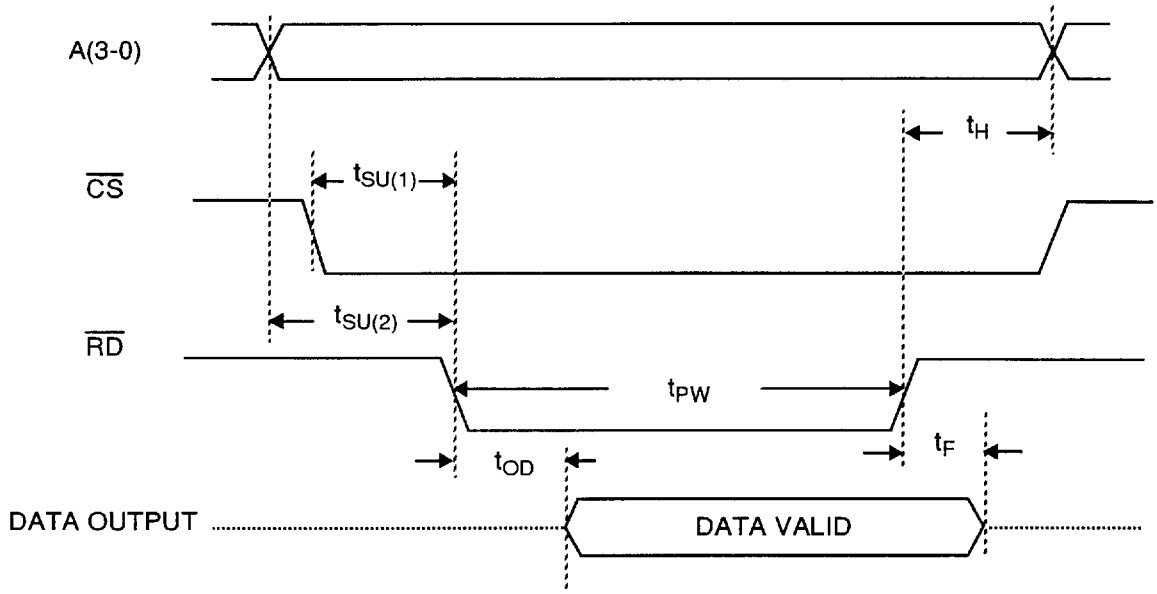
Figure 10. Microprocessor Read Timing



Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ set-up time to $\overline{RD}\downarrow$	$t_{SU(1)}$	5.0			ns
A(3-0) hold time after $\overline{RD}\uparrow$	t_H	10.0			ns
A(3-0) set-up time to $\overline{RD}\downarrow$	$t_{SU(2)}$	10.0			ns
$\overline{RD}$ pulse width	t_{PW}	38			ns
DATA output delay after $\overline{RD}\downarrow$	t_{OD}			8.0	ns
DATA float after $\overline{RD}\uparrow$	t_F			2.0	ns

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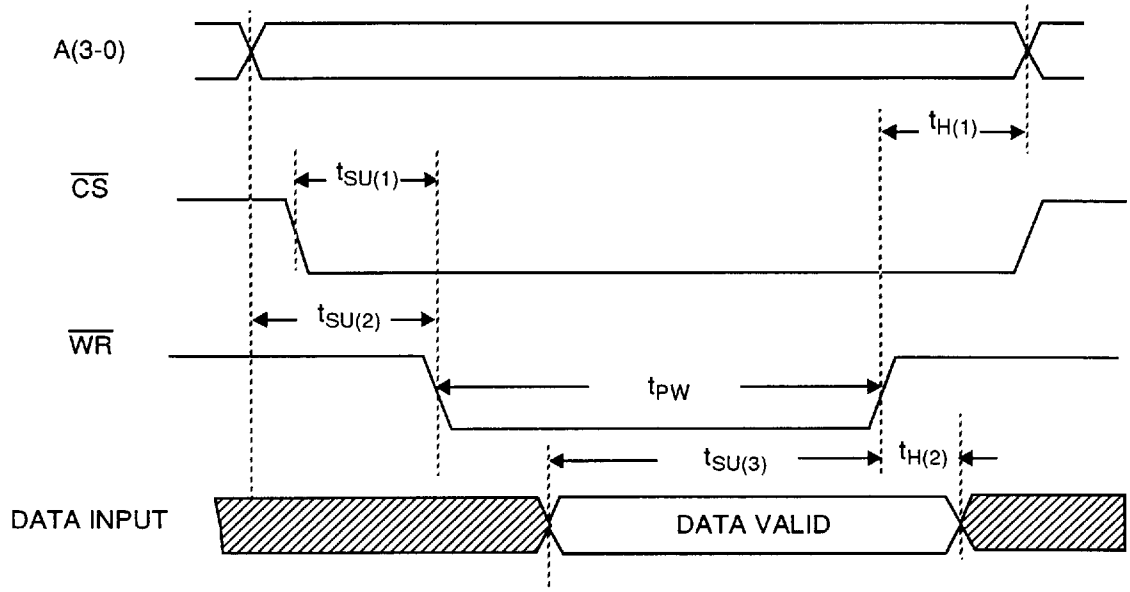
Figure 11. Microprocessor Write Timing



Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ set-up time to $\overline{WR}\downarrow$	$t_{SU(1)}$	5.0			ns
A(3-0) hold time after $\overline{WR}\uparrow$	$t_{H(1)}$	10.0			ns
A(3-0) set-up time to $\overline{WR}\downarrow$	$t_{SU(2)}$	10.0			ns
$\overline{WR}$ pulse width	t_{PW}	38			ns
DATA set-up time to $\overline{WR}\uparrow$	$t_{SU(3)}$	10.0			ns
DATA hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	5.0			ns

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OPERATION

XBERT Register Bit Map

The XBERT memory map consists of counters and register bit positions accessed by a processor read/write cycle. The unused bit position in register 01H must be masked by software to avoid reading incorrect data.

Address (Hex)	Mode*	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	R/W	POLY	PROG	SEL1	SEL0	RESET	INVTD	MODE1	MODE0
01	R/W	ERR1	ERR0	SSE	RESETC	--	TLBK	TEST	LOF
02	R/W	Programmable Word 4							
03	R/W	Programmable Word 3							
04	R/W	Programmable Word 2							
05	R/W	Programmable Word 1							
06	R	Bit Error Counter (MSB)							
07	R	Bit Error Counter							
08	R	Bit Error Counter (LSB)							
09	R	Bit Counter (MSB)							
0A	R	Bit Counter							
0B	R	Bit Counter (LSB)							

*Read/write (R/W); Read only (R); Write only (W).

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XBERT Register Bit Map Definitions

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="5">00</td><td>7
6
5
4</td><td>POLY
PROG
SEL1
SEL0</td><td>Test Pattern Generator and Detector: Bits 7 through 4 are used to select a test pattern according to the truth table shown below. The 2^{20} - 1 pseudorandom test pattern designator ZS stands for zero suppression. The 2^{20} - 1 with zero suppression is also defined as a QRSS signal. This test pattern is not supported in the byte mode. The test pattern is common for both generation and detection (Including programmable words).
<table>
<tr><th>Polynomial (POLY)</th><th>Program (PROG)</th><th>Select 1 (SEL1)</th><th>Select 0 (SEL0)</th><th>Test Pattern</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0000000000. . . .</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1111111111. . . .</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1010101010. . . .</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1100110011. . . .</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Word 1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Word 1, 2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Word 1, 2, 3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Word 1, 2, 3, 4</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>2^{15} - 1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>2^{20} - 1(ZS)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>2^{20} - 1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>2^{23} - 1</td></tr>
</table></td></tr>
<tr><td>3</td><td>RESET</td><td>Reset XBERT: A global reset occurs when a one is written to this bit position. This must be followed by writing a zero into this location. Reset clears the internal counters, generators, and detectors, as well as the control bits and performance counters in the memory map.</td></tr>
<tr><td>2</td><td>INVTD</td><td>Invert Transmit Data: A one written into this position causes the data to be inverted for transmission. The data is inverted for the bit-serial, nibble-parallel, and byte-parallel interfaces.</td></tr>
<tr><td>1
0</td><td>MODE1
MODE0</td><td>XBERT Interface Selection: The XBERT transmit and receive interface is selected according to the following table:.
<table>
<tr><th>MODE1</th><th>MODE0</th><th>Interface Selected</th></tr>
<tr><td>0</td><td>0</td><td>Bit-serial</td></tr>
<tr><td>0</td><td>1</td><td>Nibble-parallel</td></tr>
<tr><td>1</td><td>1</td><td>Byte-parallel</td></tr>
</table></td></tr>
</table>

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Address	Bit	Symbol	Description
01	7 6	ERR1 ERR0	**Transmit Error Rate:** These two bits control the generation of the fixed bit error rates given in the table below. For example, a $10E^{-3}$ error rate results in the XBERT transmitting one bit in a thousand in error. The error is generated by inverting a single bit in the bit pattern. The error rate ger tion is independent of the pattern selected (pseudorandom, fixed word pro-grammable).
	5	SSE	**Send Single Error:** A single bit error is transmitted by writing a one into this bit position. The error is sent in the next bit time after being written. After sending the single error, the bit is reset by the XBERT. The microprocessor must write a one in order to send another single bit error.
	4	RESETC	**Reset Performance Counters:** A one causes the bit error counter (locations 06H, 07H, and 08H) and the bit counter (locations 09H, 0AH, and 0BH) to reset. XBERT resets this bit after the performance counters are reset.
	3		Unused.
	2	TLBK	**Transmit Loopback:** A one activates the transmit loopback testing feature. Data is transmitted and is also looped back as receive data. The receive data input is disabled.
	1	TEST	**TranSwitch Test:** Do not use. A zero must be written into this bit position.
	0	LOF	**Loss of Frame:** For a 101010 pattern, the receive data is in frame when two consecutive 10 patterns are received correctly. Loss of frame occurs when three consecutive 10 patterns are received in error. For a 11001100 pattern, the data is in frame when two consecutive 1100 patterns are received correctly. Loss of frame occurs when three consecutive 1100 patterns are received in error. For a programmable word (locations 02H, 03H, 04H, and 05H), the receive data is in frame when two successive programmable words of length n (n = 1-4) are detected. Loss of frame occurs when three consecutive programmable words of length n are received in error. For the all pseudorandom patterns, the data is in frame when the first 24 bits in the pattern are received correctly. Loss of frame occurs when 30 bits in a thousand bits for a pattern are received in error. In all cases, the search for framing starts immediately. Loss of frame disables the bit error rate counter and the bit counter. The loss of frame alignment circuit for the pseudorandom detectors is disabled by the receive start of the pseudorandom signal ($\overline{RSF}$).

ERR1	ERR0	Error Rate
0	0	No errors
0	1	10^{-3} error rate
1	0	10^{-6} error rate

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Address	Bit	Symbol	Description
02	7-0		**Programmable Word 4:** The XBERT provides four register locations (02H, 03H, 04H, and 05H) for a microprocessor written test pattern. The number of words that comprise the programmable test pattern is selected in the 00H register location. Bit 7 in this register location is the most significant bit (MSB) and the first bit transmitted. If four bytes are selected, bit 0 in word 1 is the last bit transmitted in the test sequence. For example, the test sequence for a four-word test pattern is shown below: Word 4 Word 3 Word 2 Word 1 Word 4 ← MSBXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXLSB MSBXXXXXXX The receive detector checks the incoming data for frame alignment using the programmable pattern for frame alignment.
03	7-0		**Programmable Word 3:** The second programmable word sent. Bit 7 is the most significant bit in the word.
04	7-0		**Programmable Word 2:** The third programmable word sent. Bit 7 is the most significant bit in the word.
05	7-0		**Programmable Word 1:** The fourth programmable word sent. Bit 7 is the most significant bit in the word.
06* 07 08	7-0		**Bit Error Counter:** Register locations 06H, 07H, and 08H provide a total count of the number of bit errors that have occurred. The counter is enabled after frame alignment occurs for the test pattern selected. Bit 7 in 06H is the most significant bit, while bit 0 in 08H is the least significant bit. The counter is non-saturating and will roll-over when it becomes full. To insure that no counts are lost, all bit error counter registers plus all bit counter registers (registers 06, 07, 08, 09, 0A and 0B) are simultaneously latched when register 08 is read. If the counter registers are always read in the same order, then no counts will be lost. The counter is cleared by writing a one to bit 4 (RESETC) in 01H, or through a global reset.
09* 0A 0B	7-0		**Bit Counter:** Register locations 09H, 0AH, and 0BH provide a total count of the number of data bits that have been received. The counter is enabled after frame alignment occurs for the test pattern selected. Bit 7 in 09H is the most significant bit, while bit 0 in 0BH is the least significant bit. The counter is non-saturating and will roll-over when it becomes full. It takes approximately 0.32 seconds for the counter to roll-over for a 51.84 Mbit/s signal. To insure that no counts are lost, all bit error counter registers plus all bit counter registers (registers 06,07,08,09,0A and 0B) are simultaneously latched when register 08 is read. If the counter registers are always read in the same order, then no counts will be lost. The counter is cleared by writing a one to bit 4 (RESETC) in 01H or through a global reset.

*It is suggested that software read these registers in the following sequence: 09, 0A, 0B, 06, 07, 08.

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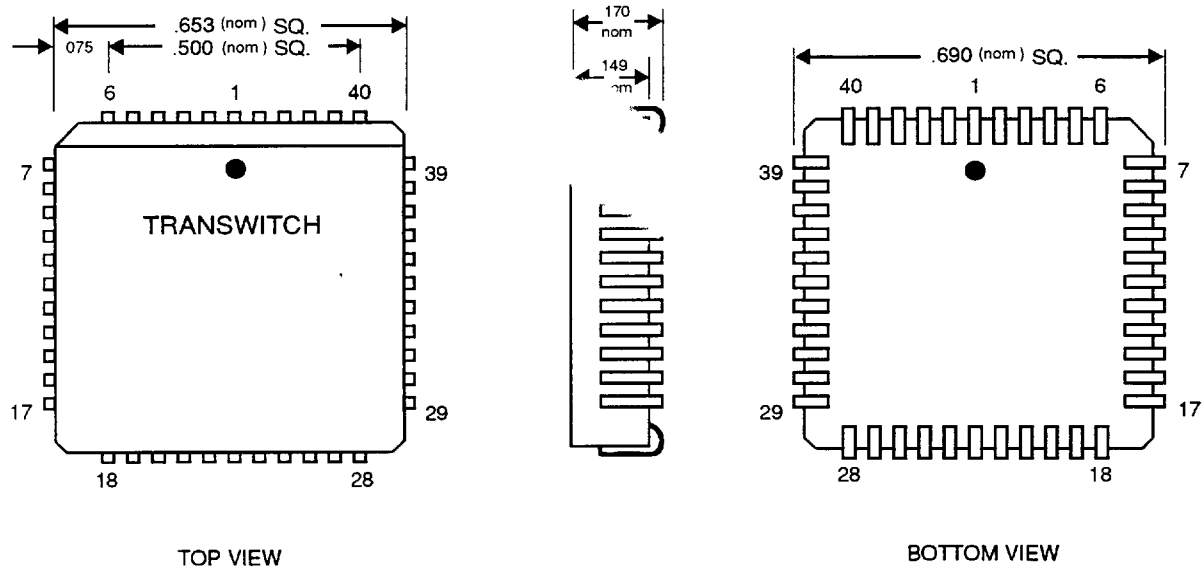
PACKAGING

The XBERT is available in a 44-pin plastic leaded chip carrier as illustrated below. All dimensions shown are in inches.



TOP VIEW

BOTTOM VIEW

Figure 12. XBERT 44-Pin Plastic Leaded Chip Carrier

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ORDERING INFORMATION

Part Number:	TXC-06125-ACPL	44-pin plastic leaded chip carrier
	TXC-06125-ACPL/B	44-pin plastic leaded chip carrier with 96-hour burn-in at 125°C

RELATED PRODUCTS

TXC-21075, XBERT Evaluation Board. A complete, ready-to-use test bed for the test and evaluation of the programmable XBERT Bit Error Rate Generator/Receiver VLSI device. Includes on-board microprocessor, RS-232 interface, and MS-DOS compatible PC software. The PC software provides full access to XBERT for custom programming, and access to the device's event and error counters. The software also determines AVG BER for comparison to external test sets.

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